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## CLAIMS

[Claims 1]

A reflective liquid crystal display in which a plurality of switching elements are formed on a semiconductor substrate and are electrically isolated from one another, a plurality of reflective pixel electrodes corresponding to the plurality of switching elements are formed on the top layer of a plurality of functional films laminated over the plurality of switching elements to form a film and are electrically isolated from one another, one pixel is formed by combining one of the reflective pixel electrode connected to one of the switching elements and a storage capacitor of the switching element, a plurality of said pixels are placed in a matrix, a transparent counter electrode is formed on the undersurface of a transparent substrate opposed to the plurality of reflective pixel electrodes, and liquid crystal is sealed between the plurality of reflective pixel electrodes and the counter electrode, the reflective liquid crystal display comprising:

at least two layers of light-blocking metallic films, wherein said films are formed between the semiconductor substrate and the plurality of reflective pixel electrodes by interposing an insulating film on and under each layer of the light-blocking metallic films in order to block part of the read light reaching a switching element when part of the read light that is made incident from a transparent substrate side to a liquid crystal through a counterelectrode penetrates a insulating film through an opening formed between the adjacent reflective pixel electrodes, one of the light-blocking metallic films of each layer covers the opening formed between the adjacent reflective pixel electrodes, and one of the light-blocking metallic films for each layer is electrically isolated from the adjacent pixel, and one of the light-blocking metallic films of each layer is electrically connected, through a via hole, to one of the switching elements, one of the reflective pixel electrodes, and storage capacitors.

[Claims 2]

The reflective liquid crystal display according to Claim 1, wherein

the storage capacitance value of the storage capacitor is the sum of the storage capacitance value of a storage capacitor consisting of a diffused capacitor electrode, an insulating film, a capacitor electrode, and a capacitor electrode contact formed on the semiconductor substrate and a storage capacitance value of a storage capacitor consisting of the two layers of light-blocking metallic films and light-blocking insulating film formed between the two layers of light-blocking metallic films.

[Claims 3]

The reflective liquid crystal display according to Claim 1, wherein

at least one of two or more layers of the light-blocking metallic films is formed by laminating TiN, Ti, or TiN/Ti wherein TiN and Ti are laminated.

[Claims 4]

A reflective liquid crystal display in which a plurality of switching elements are formed on a semiconductor substrate and are electrically isolated from one another, a plurality of reflective pixel electrodes corresponding to the plurality of switching elements are formed on the top layer of a plurality of functional films laminated over the plurality of switching elements to form a film and are electrically isolated from one another, one pixel is formed by combining one of the reflective pixel electrode connected to one of the switching elements and a storage capacitor of the switching element, a plurality of said pixels are placed in a matrix, a transparent counter electrode is formed on the undersurface of a transparent substrate opposed to the plurality of reflective pixel electrodes, and liquid crystal is sealed between the plurality of reflective pixel electrodes and the counter electrode, the reflective liquid crystal display comprising:

at least two layers of light-blocking metallic films, wherein said films are formed between the semiconductor substrate and the plurality of reflective pixel electrodes by interposing an insulating film on and under each layer of the light-blocking metallic films in order to block part of the color-image read light reaching a switching element when part of the color-image read light that is made incident from a transparent substrate side to a liquid crystal through a counterelectrode penetrates a insulating film through an opening formed between the adjacent reflective pixel electrodes, and the film thickness of the light-blocking insulating film formed between the two layers of light-blocking metallic films is set to 400 nm or thinner, which is a wavelength of B (blue) light contained in the color-image read light.

[Claims 5]

A reflective liquid crystal display in which a plurality of switching elements are formed on a semiconductor substrate and are electrically isolated from one another, a plurality of reflective pixel electrodes corresponding to the plurality of switching elements are formed on the top layer of a plurality of functional films laminated over the plurality of switching elements to form a film and are electrically isolated from one another, one pixel is formed by combining one of the reflective pixel electrode connected to one of the switching elements and a storage capacitor of the switching element, a plurality of said pixels are placed in a matrix, a transparent counter electrode is formed on the undersurface of a transparent substrate opposed to the plurality of reflective pixel electrodes, and liquid crystal is sealed between the plurality of reflective pixel electrodes and the counter electrode, the reflective liquid crystal display comprising:

at least two layers of light-blocking metallic films, wherein said films are formed between the semiconductor substrate and the plurality of reflective pixel electrodes by interposing an insulating film on and under each layer of the light-blocking metallic films in order to block a part of color-image read light reaching a switching element when part of the color-image read light that is made incident from a transparent substrate side to a liquid crystal through a counterelectrode penetrates a insulating film through an opening formed between the adjacent reflective pixel electrodes, and the light-blocking insulating film formed between the two layers of light-blocking

metallic films is composed of SiN or SiON.

## DETAILED DESCRIPTION OF THE INVENTION

[0001]

**Field of the Invention**

The present invention relates to a reflective liquid crystal display capable of reducing leaked current produced in switching elements formed on a semiconductor substrate by part of the read light. Leaked current is produced when part of the read light that is made incident from a transparent substrate side into crystal liquid passes through an opening formed between adjacent reflective pixel electrodes penetrates an insulating film adjacent to the reflective pixel electrode.

[0002]

**Prior Art**

Recently, projection liquid crystal display for displaying images on large screens has been extensively used for, as some examples, outdoor public displays, control operation displays, and high-resolution image displays conforming to hi-vision broadcast standards and SVGA computer graphics standards.

[0003]

Such projection liquid crystal displays are classified largely into transmission liquid crystal displays based on a transmission method and reflective liquid crystal displays based on a reflection method. The transmission liquid crystal displays have a drawback that a TFT (Thin Film Transistor) formed in each pixel is unable to serve as a transmission area to transmit light, and, therefore, it reduces the numerical aperture. For this reason, reflective liquid crystal displays are attracting attention.

[0004]

Generally, the above-mentioned reflective liquid crystal display is configured by forming a plurality of switching elements on a semiconductor substrate (Si substrate) and which are electrically isolated from one another, forming a plurality of reflective pixel electrodes corresponding to the plurality of switching elements on the top layer of a plurality of functional films laminated over the plurality of switching elements to form a film and which are electrically isolated from one another, forming one pixel combining one of the reflective pixel electrodes connected to one of the switching elements and a storage capacitor of the switching element, placing a plurality of said pixels on the semiconductor substrate in a matrix, forming a transparent counter electrode that is common to all pixels on the undersurface of a transparent substrate (glass substrate) as opposed to the plurality of reflective pixel electrodes, and by sealing liquid crystal between the plurality of reflective pixel electrodes and the counter electrode, whereby color-image read light is emitted from the transparent substrate by the color-image read light made incident from the transparent substrate, through the counter electrode, to the liquid crystal to change the potential difference between the counter electrode and each reflective pixel electrode for each reflective pixel electrode by the switching element in response to image signals, and by modulating the color-image read light by controlling the orientation of the liquid crystal and reflecting said light on each reflective pixel electrode.

[0005]

Fig. 1 is an enlarged sectional view showing schematically one pixel in a reflective liquid crystal

display according to the conventional embodiment 1. Fig. 2(a) is a block diagram explaining an active-matrix drive circuit in the reflective liquid crystal display according to the conventional embodiment 1. Fig. 2(b) is an enlarged view showing schematically a part X of Fig. 2(a).

[0006]

The reflective liquid crystal display 10A of the conventional embodiment 1 as shown in Fig.1 is configured to be applicable to a standard reflective projector. Among a plurality of pixels of the liquid crystal display 10A to display images, one pixel will be explained with reference to the enlarged views. A semiconductor substrate 11 serving as a base of the liquid crystal display is comprised of a p-type Si substrate (or an n-type Si substrate) such as monocrystalline silicon. At the left side of the semiconductor substrate (hereinafter referred to as p-type Si substrate) 11 in Fig.1, a p-well region 12 is formed and electrically isolated pixel by pixel by left and right field oxide films 13A and 13B. A switching element 14 is formed in the p-well region 12, which is composed as a MOSFET (Metal Oxide Semiconductor Field Effect Transistor).

[0007]

In one switching element (hereinafter referred to as MOSFET) 14, a gate G is formed by laminating a gate electrode 16 comprising polysilicon on a gate oxide film 15 formed at approximately the center of the surface of the p-well region 12.

[0008]

On the left side of the gate G of the MOSFET 14 in Fig. 1, a drain region 17 is formed, and on the drain region 17, a drain electrode 18 is laminated with aluminum wiring in a first via hole Via 1, to form a drain D.

[0009]

On the right side of the gate G of the MOSFET 14 in Fig. 1, a source region 19 is formed, and on the source region 19, a source electrode 20 is laminated with aluminum wiring in a first via hole Via 1, to form a source S.

[0010]

On the right side of the p-well region 12 on the p-type Si substrate 11 in Fig. 1, an ion-implanted diffused capacitor electrode 21 is formed. Said diffused capacitor electrode 21 is electrically isolated pixel by pixel by the left and right field oxide films 13B and 13C. A range from the field oxide film 13A to the field oxide film 13C corresponds to one pixel.

[0011]

An insulating film 22 and a capacitor electrode 23 are laminated in this order on the diffused capacitor electrode 21 and a capacitor electrode contact 24 is laminated on the capacitor elecitor 23 with aluminum wiring in a first via hole Via 1 to form a storage capacitor C corresponding to one of MOSFETs 14.

[0012]

A plurality of functional films including a first interlayer insulating film 25, a first metallic film 26, a second interlayer insulating film 27, a second metallic film 28, a third interlayer insulating film 29, and a third metallic film 30 are formed in this order over the field oxide films 13A to 13C, gate

electrode 16, and capacitor electrode 23.

[0013]

The first, second and third interlayer insulating films 25, 27, and 29 are laminated using, for example, $SiO_2$ (silicon oxide) that has insulating property.

[0014]

The first, second, and third metallic films 26, 28, and 30 comprise, for example, conductive aluminum wiring and are segmented into predetermined patterns for one pixel corresponding to one switching element 14. Within the same pixel, the first, second, and third metallic films 26, 28, and 30 are electrically connected to each other; however, the first, second, and third metallic films 26, 28, and 30 are electrically isolated from those in each adjacent pixel by forming openings 26a, 28a, and 30a in the metallic films 26, 28, and 30 between adjacent films.

[0015]

In one pixel, the lowermost first metallic film 26 is connected to the corresponding one switching element 14 and storage capacitor C through the drain electrode 18, source electrode 20, and capacitor electrode contact 24 that are formed from aluminum wiring filled in the first via holes Via 1 etched in the first interlayer insulating film 25.

[0016]

In addition, in one pixel, the intermediate second metallic film 28 serves as a light-blocking metallic film to block part of read light L made incident to an upper transparent substrate 42 (to be explained later) from reaching the MOSFET 14 formed on the lower p-type Si substrate 11. That is, the second metallic film (light-blocking metallic film) 28 is formed to cover the opening 30a formed between adjacent top third metallic films 30 in order to block part of read light L entering the opening 30a. The second metallic film 28 is connected to the lowermost first metallic film 26 through the aluminum wiring filled in the second via hole Via 2 etched in the second interlayer insulating film 27.

[0017]

In addition, in one pixel, the top third metallic film 30 is formed as one square reflective pixel electrode correspondent to one pixel. The metallic film 30 is separated from any adjacent one pixel by the opening 30a formed between them and is connected to the intermediate second metallic film 28 by laminating aluminum wiring in a third via hole Via 3 etched in the third interlayer insulating film 29.

[0018]

Liquid crystals 40 are sealed on the third metallic film (hereinafter referred to as reflective pixel electrode) 30. A transparent counter electrode 41 is laminated, through said liquid crystals 40, on the undersurface of the transparent substrate (glass substrate) 42 to face the reflective pixel electrodes 30 and serve as a common electrode for the reflective pixel electrodes 30 without being segmented into pixels. The counter electrode 41 is laminated using, for example, ITO (indium tin oxide).

[0019]

Next, the active-matrix drive circuit to drive a matrix where a plurality of above-mentioned MOSFETs (switching elements) 14 are placed on the p-type Si substrate 11 in a matrix in the reflective liquid crystal display 10A according to the conventional embodiment 1 will be explained with reference to

Figs. 2(a) and 2(b).

[0020]

As shown in Figs. 2(a) and 2(b), in the active-matrix drive circuit 70 of the reflective liquid crystal display 10A, a plurality of MOSFETs (switching elements) 14 are placed on the p-type Si substrate (semiconductor substrate) 11 in a matrix. One pixel is formed by combining one reflective pixel electrode 30 connected to the MOSFET 14 and storage capacitor C for the MOSFET, and a set of such pixels is arranged in a matrix on the p-type Si substrate 11.

[0021]

To specify one of the pixels among a plurality of pixels, a horizontal shift register circuit 71 and a vertical shift register circuit 75 are provided in column and row directions, respectively.

[0022]

First, in the horizontal shift register circuit 71, a signal line 73 is vertically wired through the video switch 72 for each column of pixels, but for the sake of convenience, only one signal line 73 connected to the horizontal shift register circuit 71 is shown. A video line 74 is connected to the signal line 73 provided between the horizontal shift register 71 and the video switch 72. One signal line 73 is connected to a plurality of drain electrodes 18 of MOSFETs 14 that are placed in one column.

[0023]

Next, in the vertical shift register circuit 75, a gate line 76 is horizontally wired for each row of pixels, but for the sake of convenience, only one gate line 76 extended from the horizontal shift register circuit 75 is shown. One gate line 76 is connected to a plurality of gate electrodes 16 of the MOSFETs 14 that are placed in one row.

[0024]

The source electrode 20 of each MOSFET 14 is connected to one of the reflective pixel electrodes 30 and the capacitor electrode contact 24 and capacitor electrode 23 of the storage capacitor C. The active-matrix drive circuit 70 employs a known flame inversion driving method that inverts the polarity of video signals between positive and negative frame by frame, that is, for example, video signals to be written in an "n"th frame period are provided with positive polarity and those to be written in an "n+1"th frame period are provided with negative polarity. Therefore, to supply a video signal from the signal line 73, the signal line 73 may be connected to one of the drain electrodes 18 or the source electrode 20 of the MOSFET 14. In this example, the signal line 73 is connected to the drain electrode 18 as mentioned above. However, if the signal line 73 is connected to the source electrode 20, the drain electrode 18 is connected to the reflective pixel electrode 30 and the capacitor electrode contact 24 and capacitor electrode 23 of the storage capacitor C.

[0025]

In the reflective liquid crystal display 10A according to above-mentioned conventional embodiment 1, it is required that a fixed well potential is supplied to the MOSFET 14, and a fixed COM (common) potential is supplied to the storage capacitor C.

[0026]

That is, the well potential to the MOSFET 14 is fixed to, for example, 15 V and is supplied between

the gate line 76 and a well potential contact on a p+ region (not shown) formed in one p-well region 12 (Fig. 1). However, if an n-type Si substrate is used, the well potential may be, for example, 0 V.

[0027]

The COM potential to the storage capacitor C is fixed to, for example, 8.5 V and is supplied between the capacitor electrode 24 of the storage capacitor C and a common potential contact (not shown) on the diffused capacitor electrode 22. In this case, the COM potential can basically be of any voltage to form the storage capacitor C. However, it may be set to a center value (for example, 8.5 V) of video signals, to make the voltage applied to the storage capacitor C about half a source voltage. That is, a storage capacitor's withstanding voltage is about half a source voltage. It is possible, therefore, to thin the film's thickness of only the insulating film 22 of the storage capacitor C, to increase the capacitance value. The larger the storage capacitance value of the storage capacitor C, the smaller the potential change the reflective pixel electrode 30 receives. This is advantageous in preventing flickering and burning.

[0028]

The storage capacitor C has a function that stores charge in accordance with the potential difference between a potential applied to one reflective pixel electrode 30 and the COM potential, keeps the stored voltage during an unselected period or OFF period of the MOSFET 14, and continuously applies the stored voltage to the reflective pixel electrode 30.

[0029]

To drive one pixel, the active-matrix drive circuit 70 of the reflective liquid crystal display 10A according to the conventional embodiment sequentially supplies video signals to the video line 74 at shifted timing. One of the video signals is supplied to the signal line 73 through the video switch 72. At this time, one MOSFET 14 located at an intersection of the signal line 73 and a selected gate line 76 is turned on.

[0030]

The video signal is supplied to the selected reflective pixel electrode 30 through the signal line 73 and is written as charge into the storage capacitor C. This causes the potential difference between the selected reflective pixel electrode 30 and the counter electrode 41 (Fig. 1) according to the video signal and modulates the optical characteristic of the liquid crystals 40. As a result, color-image read light L (Fig. 1) made incident from the transparent substrate 42 is modulated by the liquid crystals 40 pixel by pixel, reflected by the reflective pixel electrodes 30, and emitted from the transparent substrate 42. Thus, unlike the transmission mode, the reflective liquid crystal display can utilize read light L (Fig. 1) nearly 100% to provide high-resolution, high-luminance projection images.

[0031]

At this time, as shown in Fig. 1, part of the color-image read light L made incident from the transparent substrate 42 side penetrates the third interlayer insulating film 29 through the openings 30a formed between adjacent reflective pixel electrodes 30. The penetrated light is repeatedly reflected in the third interlayer insulating film 29 between the reverses of the reflective pixel electrodes (third metallic films) 30 made of aluminum wiring and the surfaces of the light-blocking metallic films

(sccond metallic films) 28 madc of aluminum wiring. Thereafter, the repcatcdly reflected light penetrates the second interlayer insulating film 27 through the openings 28a where no light-blocking metallic film 28 is formed. In the second interlayer insulating film 27, the light is repeatedly reflected betwccn the reverses of the light-blocking metallic films 28 made of aluminum wiring and the surfaces of the first metallic films 26 made of aluminum wiring. Thereafter, the repeatedly reflected light penetrates the first intcrlaycr insulating film 25 through the openings 26a where no first metallic film 26 is formed. Each opening 26a where no first metallic film 26 is laminated is located above the gate electrode 16 of the MOSFET 14 or the capacitor electrode 23 of the storage capacitor C, so the part of the read light L pcnctrating the first interlayer insulating film 25 reaches the gate electrode 16, drain region 17, souree region 19 of the MOSFET 14 and the capacitor electrode 23 of the storage capacitor C.

[0032]

If part of the read light L penetrates the drain region 17 and source region 19 of the MOSFET 14, the photodiode function works beeause there are pn junctions between the p-well region 12 and the drain region 17 and source region 19 that are comprised of high-concentration n+ impurity layers in the MOSFET 14. As a result, thc part of the read light L generates photocarriers to eause leaked current, which may vary the potential of the reflective pixel electrode 30. The variation in the potential of the refleetive pixel eleetrode 30 may cause flickering and burning. It is neeessary, therefore, to minimize light leakage to the MOSFET 14 caused by part of the read light L.

[0033]

There is a liquid crystal display employing a technique of suppressing light leakage to a MOSFET 14 due to the above-mentioned part of read light L (for example, see Patent Literature 1).

[0034]

Patent Literature 1: Japanese Unexamined Patent Application No. 2002-40482

[0035]

Fig. 3 is a sectional view showing schematically a liquid crystal display acording to the conventional embodiment 2. The liquid crystal display 100 according to the conventional embodiment 2 shown in Fig. 3 is the one disclosed in the above-mentioncd Patent Literature 1 (Japanese Unexamined Patent Application No. 2002-40482). With reference to the Patent Literature 1, the liquid crystal display 100 will be explained briefly.

[0036]

As shown in Fig. 3, the liquid crystal display 100 according to the conventional embodiment 2 is provided with a first substratc (drive circuit substrate) 101 on whieh a plurality of active elements 102 are formed. One active elcment 102 consists of a gate electrode 103, a drain region 104, and a source region 105. The drain and source regions 104 and 105 are formed on the left and right sides of the gate eleetrode 103, respectively. One aetive element 102 is eleetrieally isolated from adjaeent aetive elements 102 by left and right field oxide films 107 that are continue to an insulating film 106.

[0037]

In addition, on the aetive element 102, a plurality of funetional films ineluding a first interlayer film

108, a first conductive film 109, a second interlayer film 110, a first light-blocking film 111, a third interlayer film 112, a second light-blocking film 113, a fourth interlayer film 114, and a second conductive film (hereinafter referred to as reflective electrode) 115 serving as a reflective electrode are laminated one upon another in this order.

[0038]

The first conductive film 109, the first light-blocking film 111, the second light-blocking film 113, and the reflective electrode 115 are conductive and are sectioned into predetermined patterns to serve the active elements 102.

[0039]

The first conductive film 109 is connected to the drain region 104 and source region 105 of one active element 102 through the first via holes Via 1 formed in the first interlayer film 108. The first light-blocking film 111 must be provided with a second via hole Via 2 indicated with an imaginary line outside Fig. 3, to apply a voltage thereto. The second light-blocking film 113 is connected to the first conductive film 109 through a third via hole Via 3 formed in the second and third interlayer films 110 and 112. The reflective electrode 115 is connected to the second light-blocking film 113 through a fourth via hole Via 4 formed in the fourth interlayer film 114. Accordingly, the reflective electrode 115 is connected to the corresponding active element 102 through the second light-blocking film 113 and first conductive film 109.

[0040]

On the reflective electrodes (second conductive films) 115, an aligning film 116, a liquid crystal composition 117, an aligning film 118, a counter electrode 119, and a second substrate (transparent substrate) 120 are formed in this order. The liquid crystal composition 117 is partitioned by left and right spacers 121 for each reflective electrode 115 (one pixel).

[0041]

The spacer 121 is positioned on an opening 115a formed between adjacent reflective electrodes 115. The second light-blocking film 113 has substantially the same size as the reflective electrode 115 and is formed to cover the opening 115a. The first light-blocking film 111 is formed to cover an opening 113a formed between adjacent second light-blocking films 113. Part of read light L made incident to the second substrate (transparent substrate) 120 may penetrate the fourth interlayer film 114 through the opening 115a formed between adjacent reflective electrodes 115. The penetrated light is blocked by the first and second light-blocking films 111 and 113, so the light may not reach the active elements 102 formed on the first substrate 101. In this way, this disclosure suppresses light leakage to the active elements 102 due to the penetration of part of the read light L.

[0042]

According to the liquid crystal display 100 of the conventional embodiment 2, a voltage is applied to the first light-blocking film 111, and the first light-blocking film 111, third interlayer film 112, and second light-blocking film 113 form a capacitor. When a voltage applied to the reflective electrode 115 is changed relative to the potential of the counter electrode 119, the reflective electrode 115, liquid crystal composition 117, and counter electrode 119 form a first capacitor, and the first light-blocking

film 111, second light-blocking film 113, and second light-blocking film 113 form the second capacitor mentioned above.

[0043]

It is disclosed that this configuration prevents unnecessary light incident to the liquid crystal display elements and realizes a high-quality liquid crystal display 100 and a liquid-crystal projector employing the liquid crystal display.

[0044]

**Problems to be Solved by the Invention**

According to the reflective liquid crystal display 10A of the conventional embodiment 1 shown in Fig. 1, part of color-image read light L made incident from the transparent substrate 42 reaches the MOSFETs 14 formed on the p-type Si substrate 11, whereby light leakage occurs.

[0045]

According to the reflective liquid crystal display 100 of the conventional embodiment 2 of Fig. 3, the second light-blocking film 113 is formed under the reflective electrodes 115, to cover the opening 115a formed between the adjacent reflective electrodes 115. In addition, the second light-blocking film 113 is formed under the second light-blocking films 113, to cover the opening 113a formed between the adjacent second light-blocking films 113. This arrangement prevents part of read light L made incident to the second substrate (transparent substrate) 120 from reaching the active elements 102 formed on the first substrate 101. Therefore, no light leakage occurs. However, when forming over the first substrate 101, the first conductive film 109, second interlayer film 110, first light-blocking film 111, third interlayer film 112, second light-blocking film 113, fourth interlayer film 114, and reflective electrode (second conductive film) 115 in this order, a process of forming the first via holes Via 1 for the first conductive film 109, a process of forming the second via holes Via 2 for the first light-blocking film 111, a process of forming the third via holes Via 3 for the second light-blocking film 113, and a process of forming the fourth via holes Via 4 for the reflective electrode (second conductive film) 115 must be carried out. The increased number of via hole forming processes elongates the manufacturing time of the liquid crystal display 100 and deteriorates the yield thereof.

[0046]

It is desired that a reflective liquid crystal display that minimizes light leakage to switching elements due to part of read light L made incident from a transparent substrate with at least two layers of light-blocking metallic films that are formed between a semiconductor substrate and a reflective pixel electrode with an insulating film being laid on and under each layer of the light-blocking metallic films. The number of via-hole forming processes needed for the reflective liquid crystal display is smaller than that of the conventional embodiment 2 by one. The thickness of the light-blocking insulating film formed between the two light-blocking metallic films is set to be appropriate for color-image read light. Each switching element formed on the semiconductor substrate of the reflective liquid crystal display can have an increased storage capacitance value.

[0047]

**Means of Solving the Problems**

The present invention has been devised in consideration of the above-mentioned circumstances. The first invention is that of a reflective liquid crystal display in which a plurality of switching elements are formed on a semiconductor substrate and which are electrically isolated from one another, a plurality of reflective pixel electrodes corresponding to the plurality of switching elements are formed on the top layer of a plurality of functional films laminated over the plurality of switching elements to form a film and which are electrically isolated from one another, one pixel is formed by combining one of the reflective pixel electrodes connected to one of the switching elements and a storage capacitor of the switching element, a plurality of said pixels are placed in a matrix, a transparent counter electrode is formed on the undersurface of a transparent substrate opposed to the plurality of reflective pixel electrodes, and liquid crystal is sealed between the plurality of reflective pixel electrodes and the counter electrode, the reflective liquid crystal display comprising:

at least two layers of light-blocking metallic films, wherein said films are formed between the semiconductor substrate and the plurality of reflective pixel electrodes by interposing an insulating film on and under each layer of the light-blocking metallic films in order to block part of the read light reaching a switching element when part of the read light that is made incident from a transparent substrate side to a liquid crystal through a counterelectrode penetrates a third interlayer insulating film through an opening formed between the adjacent reflective pixel electrodes, one of the light-blocking metallic films of each layer covers the opening formed between the adjacent reflective pixel electrodes, and one of the light-blocking metallic films for each layer is electrically isolated from the adjacent pixel, and one of the light-blocking metallic films of each layer is electrically connected, through a via hole, to one of the switching elements, one of the reflective pixel electrodes, and storage capacitors.

[0048]

The second invention is that of a reflective liquid crystal display according to the abovementioned first invention,

wherein the storage capacitance value of the storage capacitor is the sum of the storage capacitance value of a storage capacitor consisting of a diffused capacitor electrode, an insulating film, a capacitor electrode, and a capacitor electrode contact formed on the semiconductor substrate and a storage capacitance value of a storage capacitor consisting of the two layers of light-blocking metallic films and light-blocking insulating film formed between the two layers of light-blocking metallic films.

[0049]

The third invention is that of a reflective liquid crystal display according to the abovementioned first invention,

wherein at least one of two or more layers of the light-blocking metallic films is formed by laminating TiN, Ti, or TiN/Ti wherein TiN and Ti are laminated.

[0050]

The fourth invention is that of a reflective liquid crystal display in which a plurality of switching elements are formed on a semiconductor substrate and are electrically isolated from one another, a plurality of reflective pixel electrodes corresponding to the plurality of switching elements are formed on the top layer of a plurality of functional films laminated over the plurality of switching elements to

form a film and are electrically isolated from one another, one pixel is formed by combining one of the reflective pixel electrode connected to one of the switching elements and a storage capacitor of the switching element, a plurality of said pixels are placed in a matrix, a transparent counter electrode is formed on the undersurface of a transparent substrate opposed to the plurality of reflective pixel electrodes, and liquid crystal is sealed between the plurality of reflective pixel electrodes and the counter electrode, the reflective liquid crystal display comprising:

at least two layers of light-blocking metallic films, wherein said films are formed between the semiconductor substrate and the plurality of reflective pixel electrodes by interposing an insulating film on and under each layer of the light-blocking metallic films in order to block part of color-image read light reaching a switching element when the part of color-image read light that is made incident from a transparent substrate to a liquid crystal through a counterelectrode penetrates a insulating film through an opening formed between the adjacent reflective pixel electrodes, and the film's thickness of the light-blocking insulating film formed between the two layers of light-blocking metallic films is set to 400 nm or thinner, which is a wavelength of B (blue) light contained in the color-image read light.

[0051]

The fifth invention is that of a reflective liquid crystal display in which a plurality of switching elements are formed on a semiconductor substrate and are electrically isolated from one another, a plurality of reflective pixel electrodes corresponding to the plurality of switching elements are formed on the top layer of a plurality of functional films laminated over the plurality of switching elements to form a film and are electrically isolated from one another, one pixel is formed by combining one of the reflective pixel electrode connected to one of the switching elements and a storage capacitor of the switching element, a plurality of said pixels are placed in a matrix, a transparent counter electrode is formed on the undersurface of a transparent substrate opposed to the plurality of reflective pixel electrodes, and liquid crystal is sealed between the plurality of reflective pixel electrodes and the counter electrode, the reflective liquid crystal display comprising:

at least two layers of light-blocking metallic films, wherein said films are formed between the semiconductor substrate and the plurality of reflective pixel electrodes by interposing an insulating film on and under each layer of the light-blocking metallic films in order to block part of color-image read light reaching a switching element when the part of color-image read light that is made incident from a transparent substrate side to a liquid crystal through a counterelectrode penetrates a insulating film through an opening formed between the adjacent reflective pixel electrodes, and the light-blocking insulating film formed between the two layers of light-blocking metallic films is composed of SiN or SiON.

[0052]

**Mode for Carrying Out the Invention**

Reflective liquid crystal displays according to the first to third embodiments of the present invention will be explained in detail with reference to Figs. 4 to 12.

[0053]

*First embodiment*

Fig. 4 is an enlarged sectional view showing schematically a pixel in a reflective liquid crystal display according to a first embodiment of the present invention.

Fig. 5 is a sectional view showing schematically an explanation of a third via hole for electrically connecting the first light-blocking metallic film (second metallic film), the second light-blocking metallic film, and the reflective pixel electrode (third metallic film), wherein Fig. 5(a) shows a diagram of the case in which the third via hole inside is formed with tungsten, and Fig. 5(b) shows a diagram of the case in which the third via hole inside is formed with aluminum wiring.

Fig. 6 is a plan view showing the reflective pixel electrode (third metallic film), second light-blocking metallic film, and third via hole shown in Fig. 4.

Fig. 7 is a sectional view for explaining the formation of storage capacitor provided for one switching element in the reflective liquid crystal display according to the first embodiment of the present invention, wherein Fig. 7(a) shows a diagram of the case of the conventional embodiment 1 as a comparison example, and Fig. 7(b) shows a diagram of the case of the present invention.

Fig. 8 is a diagram for explaining the reflectance of a light-blocking insulating film formed on the first light-blocking metallic film (second metallic film)/antireflection film in the reflective liquid crystal display according to the present invention.

[0054]

The structure of the reflective liquid crystal display 10B shown in Fig. 4 according to the first embodiment of the present invention is partially applied the technical idea of light leakage prevention of the liquid crystal display 100 of the conventional embodiment 2 previously explained with reference to Fig. 3 to the structure of the reflective liquid crystal display 10A of the conventional embodiment 1 previously explained with reference to Fig. 1. Even if at least two layers of light-blocking metallic films are formed between a semiconductor substrate and reflective pixel electrodes with an insulating film being laid on and under each layer of the light-blocking metallic films, the embodiment of the present invention can reduce the number of via-hole forming processes smaller than that of the conventional embodiment 2 by one, set the thickness of the light-blocking insulating film formed between the two layers of the light-blocking metallic films so as to provide a proper characteristic for color-image read light, and increase the storage capacitance value for each switching element formed on the semiconductor substrate.

[0055]

For convenience of explanation, components of the embodiment that are the same as those of the reflective liquid crystal display 10A of the conventional embodiment 1 explained above are represented with similar reference numerals and will be explained only when needed. Components of the embodiment that are different from those of the conventional embodiment 1 are represented with new reference numerals, and the differences from the conventional embodiment 1 will be explained mainly.

[0056]

As shown in Fig.4, the reflective liquid crystal display 10B according to the first embodiment of the

present invention has a plurality of pixels to display images. Among the pixels, one will be enlarged and explained. A semiconductor substrate 11 serving as a base is a p-type Si substrate (or an n-type Si substrate) similar to that of the reflective liquid crystal display 10A according to the conventional embodiment 1 explained with reference to Fig. 1. In the semiconductor substrate (hereinafter referred to as p-type Si substrate) 11, one p-well region 12 is formed and is electrically isolated from those in adjacent pixels by left and right field oxide films 13A and 13B. One p-well region 12 includes a switching element 14, which is a low-voltage-driven-type MOSFET. The switching element (hereinafter referred to as MOSFET) 14 has a gate G consisting of a gate electrode 16 laminated on a gate oxide film 15, a drain D consisting of a drain electrode 18 laminated on a drain region 17, and a source S consisting of a source electrode 20 laminated on a source region 19. The MOSFET 14 is so formed as to be driven at a low voltage of about 7 V.

[0057]

On the right side of the p-well region 12 on the p-type Si substrate 11, a storage capacitor C1 is formed. The storage capacitor C1 consists of a diffused capacitor electrode 21, an insulating film 22, a capacitor electrode 23, and a capacitor electrode contact 24. The storage capacitor C1 is electrically isolated from those for adjacent pixels by the left and right field oxide films 13B and 13C.

[0058]

Over the field oxide films 13A to 13C, gate electrode 16, and capacitor electrode 23, a plurality of functional films are laminated one upon another. The top functional film includes reflective pixel electrodes 30 that correspond to the MOSFETs 14, respectively, and are electrically isolated from one another pixel by pixel. Among the functional films, a first interlayer insulating film 25, the first metallic film 26, the second interlayer insulating film 27, and the second metallic film 28 are formed like those of the conventional embodiment 1. The first metallic film 26 comprises an aluminum wiring film and is connected to a corresponding switching element 14 and storage capacitor C1 through the drain electrode 18, the source electrode 20, and the capacitor electrode contact 24. The electrodes 18 and 20 and contact 24 comprise aluminum wiring filled in first via holes Via 1. The second metallic film 28 is electrically isolated by an opening 28a formed between the adjacent second metallic films 28 and is connected to the first metallic film 26 through aluminum wiring in a second via hole Via 2, similar to the conventional embodiment 1.

[0059]

The differences from the conventional embodiment 1 will be explained. The abovementioned second metallic film 28 serves as a first light-blocking metallic film to cover an opening 30a formed between adjacent reflective pixel electrodes 30 among a plurality of acent reflective pixel electrodes 30 formed over said second metallic film 28 in order to block part of color-image read light L that enters from the opening 30a and advances toward the p-type Si substrate 11.

[0060]

As shown in the enlarged views of Figs. 5(a) and 5(b), a second light-blocking metallic film 33 is laminated over the second metallic film (hereinafter referred to as first light-blocking metallic film) 28 with an antireflection film 31 and a light-blocking insulating film 32 having a predetermined film

thickness (400 nm or thinner) being interposed. The second light-blocking metallic film 33 covers the opening 28a (Fig. 4) formed between adjacent first light-blocking metallic films 28.

[0061]

A third interlayer insulating film 29 is laminated on the second light-blocking metallic film 33, and an antireflection film 34 is formed on the third interlayer insulating film 29. On the antireflection film 34, the reflective pixel electrodes (third metallic films) 30 are formed. For convenience of viewing the drawings, the antireflection films 31 and 34 are not shown in Fig. 4 and are shown in enlarged views in Figs. 5(a) and 5(b).

[0062]

The antireflection film 31 laminated on the surface of the first light-blocking metallic film (second metallic film) 28 and the antireflection film 34 laminated on the undersurface of the reflective pixel electrode (third metallic film) 30 comprise conductive TiN (titanium nitride) to prevent reflection of part of the color-image read light L that penetrates the third interlayer insulating film 29 through the opening 30a (Fig. 4) formed between adjacent reflective pixel electrodes 30.

[0063]

The light-blocking insulating film 32 is an essential part of the present invention and is usually laminated using an oxide film such as an $SiO_2$ (silicon oxide) film on the first light-blocking metallic film (second metallic film) 28/the antireflection film 31. Instead of $SiO_2$, SiN (silicon nitride) or SiON (silicon oxide nitride) having a larger dielectric constant than $SiO_2$ may be used to form the light-blocking insulating film 32.

[0064]

The thickness of the light-blocking insulating film 32 is preferably 400 nm or thinner, more preferably, about 300 nm. The reason of this is because the reflective liquid crystal display 10B reflects, by the reflective pixel electrodes 30, color-image read light L having wavelengths of 400 nm to 700 nm in a visible light range. Accordingly, there is no need of light having a B (blue) light wavelength of 400 nm or shorter in the color-image read light L, so it is not necessary to produce light having a wavelength of 400 nm or shorter in the transparent substrate 42.

[0065]

For this reason, the thickness of the light-blocking insulating film 32 is set to be equal to or thinner than the B (blue) light wavelength of 400 nm in color-image read light L, whereby part of the color-image read light L penetrated the light-blocking insulating film 32 through the openings 33a formed between adjacent second light-blocking metallic films 33 is absorbed or reflected by the first and second light-blocking metallic films 28 and 33 formed on and under the light-blocking insulating film 32. This results in further improving the light-blocking effect of the light-blocking insulating film 32.

[0066]

The light-blocking insulating film 32 is formed by chemical vapor deposition (CVD), and therefore, involves little in-plane variations on a wafer as is known. Accordingly, the thickness of the light-blocking insulating film 32 formed between the first and second light-blocking metallic films 28

and 33 can be set relatively uniformly to 400 nm or thinner. This results in reducing variation in the light-blocking effect of the light-blocking insulating film 32.

[0067]

The second light-blocking metallic film 33 formed on the light-blocking insulating film 32 is also an essential part of the present invention. It is important to form the second light-blocking metallic film 33 from metal having a low reflectance so that it may absorb part of color-image read light L that penetrates the third interlayer insulating film 29 through the openings 30a between adjacent reflective pixel electrodes 30. More precisely, the second light-blocking metallic film 33 is formed from TiN (titanium nitride), Ti (titanium), or TiN/Ti (layered TiN and Ti) to a thickness in the range of 50 nm to 200 nm. As a result, when absorbing part of the read light L with the second light-blocking metallic film 33, the reflectance of the second light-blocking metallic film 33 can be set to a low value to absorb part of the read light L entering from the openings 30a formed between adjacent reflective pixel electrodes 30.

[0068]

In addition, one reflective pixel electrode (third metallic film) 30 is connected to the corresponding first light-blocking metallic film (second metallic film) 28 formed under the reflective pixel electrode 30 through a third via hole Via 3. When forming this third via hole Via 3, the second light-blocking metallic film 33 comprises light absorbing metal for which an etching process is executable when etching the third interlayer insulating film 29. As a result, even if the second and first light-blocking metallic films 33 and 28 are formed under the reflective pixel electrode 30, the number of via-hole forming processes can be reduced by one compared with the conventional embodiment 2. Therefore, the via-hole forming processes can be three, i.e., a first via hole Via 1 forming process, a second via hole Via 2 forming process, and a third via hole Via 3 forming process.

[0069]

At this time, the resistance value of the second light-blocking metallic film 33 is higher than those of the first to third metallic films 26, 28, and 30 comprised of aluminum wiring. However, there is no need to lower the resistance value of the second light-blocking metallic film 33 because the aim of the film 33 is to block light and form a storage capacitor, which will be explained later, and the film 33 is not required to have a function of wiring to pass current. Therefore, the high resistance of the second light-blocking metallic film 33 causes no adverse effect on electric characteristics, and the film 33 functions sufficiently to meet the above-mentioned aim.

[0070]

As shown in Fig. 6, the shape of the second light-blocking metallic film 33 in each pixel is square, which is a size smaller than the square reflective pixel electrode (third metallic film) 30, and is electrically isolated pixel by pixel similar to the reflective pixel electrode 30. To separate the second light-blocking metallic film 33 pixel by pixel, the opening 33a is formed between adjacent second light-blocking metallic films 33 as shown in Fig. 4. At this time, the first light-blocking metallic films 28 cover the openings 30a formed between adjacent reflective pixel electrodes 30 as mentioned above, and therefore, there will be no problem even if the openings 33a formed between adjacent second

light-blocking metallic films 33 substantially agree with the openings 30a formed between adjacent reflective pixel electrodes 30.

[0071]

According to the first embodiment, the first light-blocking metallic films 28 cover the openings 30a formed between adjacent reflective pixel electrodes 30. It is possible to make any one of the layers of the first and second light-blocking metallic films 28 and 33 cover the openings 30a formed between adjacent reflective pixel electrodes 30. In this case, the positions of the first and second light-blocking metallic films 28 and 33 relative to the positions of the reflective pixel electrodes 30 may slightly be shifted from those shown in the Figure, and the positions of the second and third via holes Via 2 and Via 3 may slightly be shifted from those shown in the Figure.

[0072]

As mentioned above, the first and second light-blocking metallic films 28 and 33 are provided between the p-type Si substrate 11 and the reflective pixel electrodes 30, so part of color-image read light L made incident from the transparent substrate 42 side and penetrating the third interlayer insulating film 29 through the openings 30a formed between adjacent reflective pixel electrodes 30 may simply repeatedly be reflected and absorbed in the third interlayer insulating film 29 by the reflective pixel electrodes 30 and the second light-blocking metallic films 33 formed on and under the third interlayer insulating film 29, as indicated with dotted lines in Fig. 4. Therefore, part of the read light L does not reach the MOSFETs 14 formed on the p-type Si substrate 11. This configuration suppresses light leakage in the MOSFETs 14 due to part of read light L.

[0073]

As shown in Figs. 5(a) and 6, one reflective pixel electrode (third metallic film) 30 and one first light-blocking metallic film (second metallic film) 28 in a given pixel are electrically connected to each other by etching the third interlayer insulating film 29 comprised of $SiO_2$ from the position corresponding to the approximately center of the reflective pixel electrode 30. Further, the second light-blocking metallic film 33 comprised of conductive TiN, Ti, or TiN/Ti, the light-blocking insulating film 32 comprised of $SiO_2$, SiN, or SiON, and the antireflection film 31 comprised of conductive TiN are simultaneously etched to form the third via hole Via 3. The third via hole Via 3 is laminated and buried with conductive tungsten 35 by CVD method. As a result, a lower end of the tungsten 35 is electrically connected to the first light-blocking metallic film (second metallic film) 28, an intermediate part of the tungsten 35 is electrically connected to the second light-blocking metallic film 33, and an upper end of the tungsten 35 is electrically connected to the reflective pixel electrode 30 through the antireflection film 34 comprised of conductive TiN.

[0074]

Generally, an oxide film etching apparatus (not shown) is designed to etch only oxide films, and therefore, an etching rate of the apparatus for Al (aluminum) is low. Thus, the etching apparatus is designed to carry out selective etching. However, the oxide film etching apparatus can easily etch the third via hole Via 3, and at the same time, TiN, Ti, or TiN/Ti of the second light-blocking metallic film 33.

[0075]

After forming the third via hole Via 3, it is not necessarily required to bury the third via hole Via 3 with the tungsten 35. For example, as shown in Fig. 5(b), the third interlayer insulating film 29 may be etched from the position substantially corresponding to the center of the reflective pixel electrode 30, and the second light-blocking metallic film 33, light-blocking insulating film 32, and antireflection film 31 may simultaneously be etched to form the third via hole Via 3. Thereafter, a standard spattering process is employed to form an antireflection film 34 of TiN and a reflective pixel electrode 30 of aluminum wiring in the third via hole Via 3. This results in electrically connecting the reflective pixel electrode 30, second light-blocking metallic film 33, and first light-blocking metallic film 28 to one another in each pixel.

[0076]

In this way, the third via hole Via 3 has a role of electrically connecting the reflective pixel electrode (third metallic film) 30, second light-blocking metallic film 33, and first light-blocking metallic film (second metallic film) 28. As a result, the second light-blocking metallic film 33 needs no dedicated via hole, to simplify processes including lithography and etching processes.

[0077]

Next, a formation of the storage capacitor for one MOSFET 14 will be explained in connection with the conventional embodiment 1 as an example for comparison and the present invention with reference to Figs. 7(a) and 7(b).

[0078]

In Fig. 7(a), which is an example for comparison, the conventional embodiment 1 provides the MOSFET 14 formed on the p-type Si substrate 11 with the single storage capacitor C consisting of the diffused capacitor electrode 21, insulating film 22, capacitor electrode 23, and capacitor electrode contact 24 formed on the p-type Si substrate 11.

[0079]

On the other hand, the present invention of Fig. 7(b) forms the storage capacitor C1 composed of the diffused capacitor electrode 21, insulating film 22, capacitor electrode 23, and capacitor electrode contact 24 on the p-type Si substrate 11. In addition, the present invention forms the second light-blocking metallic film 33 over the first light-blocking metallic film (second metallic film) 28/antireflection film 31 (Fig. 5) through the light-blocking insulating film 32. As a result, storage capacitors C2 and C3 are formed between the first light-blocking metallic film (second metallic film) 28 and the second light-blocking metallic film 33 on the left and right sides of the third via hole Via 3. The reflective pixel electrode (third metallic film) 30, second light-blocking metallic film 33, and first light-blocking metallic film (second metallic film) 28 are electrically connected to one MOSFET 14 and the storage capacitors C1 to C3.

[0080]

If SiN or SiON having a large dielectric constant is used for the light-blocking insulating film 32, the storage capacitance value of each of the storage capacitors C2 and C3 will increase. For example, the light-blocking insulating film 32 may be made of SiN having a dielectric constant of 9. The

light-blocking insulating film 32 may be comprised of $SiO_2$ having a dielectric constant of 4.2. The light-blocking insulating film 32 comprised of SiN can increase the storage capacitance value two times or greater than that comprised of $SiO_2$.

[0081]

According to the present invention, the three storage capacitors C1 to C3 can increase the total storage capacitance value greater than that of the conventional embodiment 1, to reduce potential variations at the reflective pixel electrodes 30 and prevent flickering and burning.

[0082]

Fig. 8 shows reflectance values of SiN and $SiO_2$ films each laminated as the light-blocking insulating film 32 on the first light-blocking metallic film (second metallic film) 28/antireflection film 31 (Fig. 5). As a reference example, reflectance values of only the first light-blocking metallic film (second metallic film) 28 comprised of aluminum wiring are also shown. It is understood from Fig. 8 that the light-blocking insulating film made of SiN can decrease reflectance lower than that made of $SiO_2$. Accordingly, light-blocking effect will increase by using SiN or SiON instead of $SiO_2$ for the light-blocking insulating film 32. $SiO_2$ has a refractive index of 1.45, while SiN has a refractive index of about 2.0, and SiON has a refractive index of about 1.8 each being higher than that of $SiO_2$. A combination of the light-blocking insulating film 32 having such a high refractive index and the second light-blocking metallic film 33 having a light absorbing capability further increases the light-blocking effect.

[0083]

The operation of the reflective liquid crystal display 10B according to the first embodiment of the present invention having the above-mentioned configuration is substantially the same as that of the reflective liquid crystal display 10A according to the conventional embodiment 1 explained with reference to Figs. 2(a) and 2(b), and thus, the explanation thereof will be omitted. According to the present invention, the source electrode 20 (or drain electrode 18) of the MOSFET (switching element) 14 is connected to the three storage capacitors C1 to C3. Therefore, the sum of storage capacitance values of the storage capacitors C1 to C3 is applied between the source electrode 20 (or drain electrode 18) and the common potential COM. This is different from the conventional embodiment 1.

[0084]

A method of manufacturing the reflective liquid crystal display 10B according the first embodiment of the present invention will be explained with reference to Figs. 9(a) to 9(d) and Figs. 10(a) to 10(c) in order of processes of the method.

[0085]

Figs. 9(a) to (d) are sectional views showing the first to fourth processes of a method for manufacturing the reflective liquid crystal display according to the first embodiment of the present invention.

Figs. 10(a) to (c) are sectional views showing the fifth to seventh processes of a method for manufacturing the reflective liquid crystal display according to the first embodiment of the present invention.

[0086]

In the first process of Fig. 9(a), known techniques are employed to form a MOSFET (switching element) 14, a storage capacitor C1, and field oxide films 13A to 13C on a p-type Si substrate (semiconductor substrate) 11. Over them, sequentially laminated are a first interlayer insulating film 25, a first metallic film 26, a second interlayer insulating film 27, and a first light-blocking metallic film (second metallic film) 28/antireflection film 31 (shown only in Fig. 5). At this time, the first metallic film 26 is electrically connected to the MOSFET 14 and storage capacitor C1 through aluminum wiring in a first via holes Via 1, and the first light-blocking metallic film (second metallic film) 28 is electrically connected to the first metallic film 26 through aluminum wiring in a second via hole Via 2. Openings 28a are formed by lithography patterning and etching in the first light-blocking metallic film (second metallic film) 28/antireflection film 31 (Fig. 5), to segment and electrically isolate the first light-blocking metallic film (second metallic films) 28 pixel by pixel.

[0087]

In the second process of Fig. 9(b), a light-blocking insulating film 32 is laminated on the first light-blocking metallic film (second metallic film) 28/antireflection film 31 (Fig. 5) from $SiO_2$, SiN, or SiON to a thickness of, for example, 300 nm by CVD.

[0088]

In the third process of Fig. 9(c), a second light-blocking metallic film 33 is laminated on the light-blocking insulating film 32 from TiN, Ti, or TiN/Ti to a thickness of, for example, 70 nm by spattering. Openings 33a are formed in the light-blocking metallic film 33 by lithography patterning and etching, to segment and electrically isolate one second light-blocking metallic film 33 pixel by pixel.

[0089]

In the fourth process of Fig. 9(d), a third interlayer insulating film 29 is laminated on the second light-blocking metallic film 33 from $SiO_2$ to a thickness of, for example, 700 nm. The surface of the third interlayer insulating film 29 is flattened by, for example, chemical mechanical polishing (CMP).

[0090]

In the fifth process of Fig. 10(a), the third via holes Via 3 are formed in the third interlayer insulating film 29 by lithography patterning and etching. At this time, the second light-blocking metallic film 33 and light-blocking insulating film 32 are simultaneously etched up to the first light-blocking metallic film (second metallic film) 28. Because the second light-blocking metallic film 33 is comprised of TiN, Ti, or TiN/Ti, it can easily be etched with an oxide film etching apparatus (not shown).

[0091]

In the sixth process of Fig. 10(b), the third via holes Via 3 is laminated with a film of tungsten 35 from above the third interlayer insulating film 29 by CVD. The tungsten 35 is buried in the third via holes Via 3 by back-etching and CMP. Instead of that, it is possible to spatter aluminum in the third via holes Via 3 and etch back the aluminum to bury the same tungsten 35 in the third via holes Via 3. As a result, the tungsten 35 or aluminum is electrically connected to one second light-blocking metallic film 33 and one first light-blocking metallic film (second metallic film) 28.

[0092]

In the sixth process of Fig. 10(c), an antireflection film 34 (shown only in Fig. 5)/reflective pixel electrode (third metallic film) 30 is laminated on the third interlayer insulating film 29 by aluminum spattering. Openings 30a are formed in the reflective pixel electrodes 30 by lithography patterning and etching to segment and electrically isolate the reflective pixel electrode 30 pixel by pixel. At this time, the antireflection film 34 (Fig. 5)/reflective pixel electrode (third metallic film) 30 is electrically connected to the tungsten 35 or aluminum in the third via hole Via 3. This completes the formation of the functional films on the p-type Si substrate 11.

[0093]

The configuration of the embodiment prevents light leakage to the MOSFETs 14 more efficiently than that of the conventional embodiment 1, to realize finer pixels. Accordingly, the present invention can form more pixels in a given screen area than the conventional embodiment 1, to realize high resolution.

[0094]

The present invention can reduce the number of via-hole forming processes by one compared with the conventional embodiment 2, even if the first and second light-blocking metallic films 28 and 33 with the insulating films 27, 32, and 29 on and under the films 28 and 33 are formed between the p-type Si substrate 11 and the reflective pixel electrodes 30. In addition, the present invention connects the second light-blocking metallic film 33 to the MOSFET 14, storage capacitors C1 to C3, and reflective pixel electrode 30 through the first and second metallic films 26 and 28 formed on and under the second light-blocking metallic film 33 when forming the via holes. This configuration can increase a storage capacitance value for each MOSFET 14.

[0095]

***Second embodiment***

Fig. 11 is an enlarged sectional view showing schematically one pixel in a reflective liquid crystal display according to a second embodiment of the present invention.

[0096]

The reflective liquid crystal display 10C according to the second embodiment of the present invention of Fig. 11 is realized by partly changing the locations of the first and second light-blocking metallic films of the reflective liquid crystal display 10B of the first embodiment of the present invention. Only the difference of the second embodiment from the first embodiment will be explained briefly.

[0097]

According to the second embodiment, no light-blocking metallic film over a first light-blocking metallic film (second metallic film) 28 is formed. Instead, a second light-blocking metallic film 37 over a first metallic film 26 with a light-blocking insulating film 36 is formed. Due to this, the first light-blocking metallic film 28 over the second light-blocking metallic film 37 with a second interlayer insulating film 27 is formed. The first light-blocking metallic film 28 covers the openings 30a formed between adjacent reflective pixel electrodes 30 formed over the first light-blocking metallic film 28.

[0098]

The names of the first and second light-blocking metallic films 28 and 37 have no corresponding order of lamination of these films. The same reference numeral is allocated for the first light-blocking metallic film that is formed at the same position as the first light-blocking metallic film of the first embodiment.

[0099]

According to the second embodiment, no light-blocking metallic film is laminated over the first light-blocking metallic film (second metallic film) 28, and thus, there is only one storage capacitor C on a p-type Si substrate 11, similar to the conventional embodiment 1 explained with reference to Fig. 1.

[0100]

The light-blocking insulating film 36 mentioned above is laminated from $SiO_2$, SiN, or SiON to a thickness of 400 nm or thinner. The second light-blocking metallic film 37 mentioned above is formed from TiN, Ti, or TiN/Ti having a low reflectance to a thickness in the range of 50 nm to 200 nm.

[0101]

According to the second embodiment, when a second via hole Via 2 is formed to connect the first light-blocking metallic film (second metallic film) 28 to the first metallic film 26, tungsten or aluminum in the second via hole Via 2 electrically connects the first light-blocking metallic film 28, second light-blocking metallic film 37, and first metallic film 26 to one another. Accordingly, the second embodiment is also capable of reducing the number of via-hole forming processes by one compared with the conventional embodiment 2. Therefore, the second embodiment can reduce the number of via-hole forming processes to three to form the first to third via holes Via 1 to Via 3.

[0102]

According to the reflective liquid crystal display 10C of the second embodiment having the above-mentioned arrangement, part of the color-image read light L made incident from a transparent substrate 42 side may penetrate a third interlayer insulating film 29 through the openings 30a formed between adjacent reflective pixel electrodes 30. The penetrated light is repeatedly reflected in the third interlayer insulating film 29 between the undersurface of the reflective pixel electrodes 30 made of aluminum wiring and the surfaces of the first light-blocking metallic films 28 made of aluminum wiring. Thereafter, part of the read light L penetrates the second interlayer insulating film 27 through openings 28a formed between adjacent first light-blocking metallic films 28. Then, part of the read light L is repeatedly reflected and absorbed in the second interlayer insulating film 27 by the upper and lower first and second light-blocking metallic films 28 and 37 as indicated with dotted lines in Fig. 11. Therefore, part of the read light L never reaches the MOSFETs 14 formed on the p-type Si substrate 11. In this way, the second embodiment prevents light leakage to the MOSFETs 14 due to part of the read light L.

[0103]

***Third embodiment***

Fig. 12 is an enlarged sectional view showing schematically one pixel in a reflective liquid crystal display according to a third embodiment of the present invention.

[0104]

The reflective liquid crystal display 10D according to the third embodiment of the present invention of Fig.12 is a combination of the light-blocking metallic films of the reflective liquid crystal displays 10B and 10C according to the first and second embodiments of the present invention. Only the difference of the third embodiment from the first and second embodiments will be explained briefly.

[0105]

Like the second embodiment, the third embodiment laminates a second light-blocking metallic film 37 over a light-blocking insulating film 36 that is formed on a first metallic film 26. In addition, like the first embodiment, the third embodiment laminates a third light-blocking metallic film 39 over a light-blocking insulating film 38 formed on a first light-blocking metallic film (second metallic film) 28. The third light-blocking metallic film 39 covers openings 28a formed between adjacent first light-blocking metallic films 28.

[0106]

The names of the first, second, and third light-blocking metallic films 28, 37, and 39 do not correspond to the order of lamination of these films. The same reference numerals are allocated for the first and second light-blocking metallic films that are formed at the same positions as the first and second light-blocking metallic films of the first and second embodiments. The third light-blocking metallic film that is formed at the position of the second light-blocking metallic film of the first embodiment is provided with a different reference numeral.

[0107]

The light-blocking insulating films 36 and 38 are comprised of $SiO_2$, SiN, or SiON each to a thickness of 400 nm or thinner. The second and third light-blocking metallic films 37 and 39 are comprised of TiN, Ti, or TiN/Ti each to a thickness in the range of 50 nm to 200 nm.

[0108]

According to the third embodiment, when a second via hole Via 2 is formed in each pixel to connect the first light-blocking metallic film (second metallic film) 28 to the first metallic film 26, tungsten or aluminum in the second via hole Via 2 electrically connects the first light-blocking metallic film 28, second light-blocking metallic film 37, and first metallic film 26 to one another. When a third via hole Via 3 is formed in each pixel to connect a reflective pixel electrode (third metallic film) 30 to the first light-blocking metallic film (second metallic film) 28, tungsten or aluminum in the third via hole Via 3 electrically connects the reflective pixel electrode 30, the third light-blocking metallic film 39, and first light-blocking metallic film 28 to one another. As a result, the third embodiment is also capable of reducing the number of via-hole forming processes by one compared with the conventional embodiment 2. Therefore, the third embodiment can reduce the number of via-hole forming processes to three to form the first to third via holes Via 1 to Via 3.

[0109]

The third embodiment can further suppress light leakage to MOSFETs 14 due to part of color-image read light L than the first and second embodiments. Naturally, the third embodiment provides a storage capacitor C1 formed on a p-type Si substrate 11 similar to the first embodiment, as well as

storage capacitors C2 and C3 formed between the first light-bloeking metallic film (second metallic film) 28 and the third light-bloeking metallie film 39 on the left and right sides of the third via hole Via 3. The three storage eapaeitors C1 to C3 provide a greater total capaeitanee value than the capacitor of the convcntional embodiment 1, to suppress potential variations at the reflective pixel eleetrodes 30 and prevent flickering and burning.

[0110]

As mentioned above, eaeh of the first to third embodiments forms at least two light-bloeking metallie films between the p-type Si substrate 11 and the reflective pixel eleetrodes 30 with an insulating film being laid on and under each of the light-blocking metallic films. The number of via-hole forming proeesses involved in eaeh of the embodiments is smaller than that of the related art 2 by one. When forming via holes, the embodiments ean eonneet the light-bloeking metallie films to the MOSFET 14, storage eapacitors C1 to C3 (or C1), and reflective pixel electrode 30 through the metallic films formed on and under the light-blocking metallic films. In addition, the embodiments can provide each MOSFET 14 with a larger storage capacitanee value.

[0111]

**Effects of the Invention**

In a reflective liquid crystal display relating to the present invention explained in detail above, aecording to Claim 1, beeause the refleetive liquid erystal display comprising at least two layers of light-bloeking metallic films, wherein said films are formed between the semieonductor substrate and the plurality of reflective pixel eleetrodes by interposing an insulating film on and under each layer of the light-bloeking metallie films in order to bloek part of the read light reaehing a switching element when part of the read light that is made ineident from a transparent substrate side to a liquid crystal through a eountereleetrode penetrates a third interlayer insulating film through an opening formed between the adjacent reflective pixel electrodes, one of the light-blocking metallic films of eaeh layer covers the opening formed between the adjaeent refleetive pixel eleetrodes, and one of the light-bloeking metallie films for eaeh layer is eleetrieally isolated from the adjaeent pixel, and one of the light-bloeking metallie films of eaeh layer is electrieally eonnected, through a via hole, to one of the switching elements, one of the refleetive pixel electrodes, and storage capacitors, the number of via-hole forming processes needed for the reflective liquid crystal display is smaller than that of the eonventional embodiment 2 by one, and thus the via-hole forming proeesses ean be three, i.e., a first via hole Via 1 forming proeess, a seeond via hole Via 2 forming proeess, and a third via hole Via 3 forming proeess.

[0112]

Aeeording to Claim 2, in the reflective liquid erystal display according to Claim 1, because the storage eapaeitanee value of the storage eapaeitor is the sum of the storage capacitanee value of a storage capacitor eonsisting of a diffused capaeitor electrode, an insulating film, a capacitor electrode, and a capacitor electrode contact formed on the semieonductor substrate and a storage eapaeitanee value of a storage eapaeitor eonsisting of the two layers of light-blocking metallie films and light-blocking insulating film formed between the two layers of light-bloeking metallie films, the sum of the storage

capacitance valuc can be set larger, to reduce potential variations at the reflective pixel electrodes and prevent flickering and burning.

[0113]

According to Claim 3, in the reflective liquid crystal display according to Claim 1, because at least one of two or more layers of the light-blocking metallic films is formed by laminating TiN, Ti, or TiN/Ti wherein TiN and Ti are laminated, the reflectance of the second light-blocking metallic film can be set to a low value to absorb part of read light entering from the openings formed between adjacent reflective pixel electrodes.

[0114]

According to Claim 4, because the reflective liquid crystal display comprising at least two layers of light-blocking metallic films, wherein said films are formed between the semiconductor substrate and the plurality of reflective pixel electrodes by interposing an insulating film on and under each layer of the light-blocking metallic films in order to block part of color-image read light reaching a switching element when the part of color-image read light that is made incident from a transparent substrate side to a liquid crystal through a counterelectrode penetrates a third interlayer insulating film through an opening formed between the adjacent reflective pixel electrodes, and the film thickness of the light-blocking insulating film formed between the two layers of light-blocking metallic films is set to 400 nm or thinner, which is a wavelength of B (blue) light contained in the color-image read light, there is no need of light having a B (blue) light wavelength of 400 nm or shorter in the color-image read light, and thus the light-blocking effect of the light-blocking insulating film can be further improved.

[0115]

According to Claim 5, because the reflective liquid crystal display comprising at least two layers of light-blocking metallic films, wherein said films are formed between the semiconductor substrate and the plurality of reflective pixel electrodes by interposing an insulating film on and under each layer of the light-blocking metallic films in order to block part of color-image read light reaching a switching element when the part of color-image read light that is made incident from a transparent substrate side to a liquid crystal through a counterelectrode penetrates a third interlayer insulating film through an opening formed between the adjacent reflective pixel electrodes, and the light-blocking insulating film formed between the two layers of light-blocking metallic films is composed of SiN or SiON, light-blocking function of the part of read light entering from the openings formed between adjacent reflective pixel electrodes can be increased by SiN or SiON with low reflectance, and a storage capacitance value of a storage capacitor consisting of the two layers of light-blocking metallic films and light-blocking insulating film formed between the two layers of light-blocking metallic films can be increased by SiN or SiON with high reflectance. In addition, a combination of the light-blocking insulating film comprised of SiN or SiON having such a high refractive index and the light-blocking metallic film having a light absorbing capability further increases the light-blocking effect.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an enlarged sectional view showing schematically one pixel in a reflective liquid crystal

display according to the conventional embodiment 1.

Fig. 2(a) is a block diagram explaining an active-matrix drive circuit in the reflective liquid crystal display according to the conventional embodiment 1.

Fig. 2(b) is an enlarged view showing schematically a part X of Fig. 2(a).

Fig. 3 is a sectional view showing schematically a liquid crystal display according to the conventional embodiment 2.

Fig. 4 is an enlarged sectional view showing schematically a pixel in a reflective liquid crystal display according to a first embodiment of the present invention.

Fig. 5 is a partially enlarged sectional view showing schematically an explanation of a third via hole for electrically connecting the first light-blocking metallic film (second metallic film), the second light-blocking metallic film, and the reflective pixel electrode (third metallic film), wherein

Fig. 5(a) shows a diagram of the case in which the third via hole inside is formed with tungsten, and

Fig. 5(b) shows a diagram of the case in which the third via hole inside is formed with aluminum wiring.

Fig. 6 is a plan view showing the reflective pixel electrode (third metallic film), second light-blocking metallic film, and third via hole shown in Fig. 4.

Fig. 7 is a sectional view for explaining the formation of storage capacitor provided for one switching element in the reflective liquid crystal display according to the first embodiment of the present invention, wherein

Fig. 7(a) shows a diagram of the case of the conventional embodiment 1 as a comparison example, and

Fig. 7(b) shows a diagram of the case of the present invention.

Fig. 8 is a diagram for explaining the reflectance of a light-blocking insulating film formed on the first light-blocking metallic film (second metallic film)/antireflection film in the reflective liquid crystal display according to the first embodiment of the present invention.

Figs. 9(a) to (d) are sectional views showing the first to fourth processes of a method for manufacturing the reflective liquid crystal display according to the first embodiment of the present invention.

Figs. 10(a) to (c) are sectional views showing the fifth to seventh processes of a method for manufacturing the reflective liquid crystal display according to the first embodiment of the present invention.

Fig. 11 is an enlarged sectional view schematically showing one pixel in a reflective liquid crystal display according to a second embodiment of the present invention.

Fig. 12 is an enlarged sectional view schematically showing one pixel in a reflective liquid crystal display according to a third embodiment of the present invention.

**DESCRIPTION OF THE NUMERALS**

10B—Reflective liquid crystal display of the first embodiment according to the present invention

10C—Reflective liquid crystal display of the second embodiment according to the present invention

10D—Reflective liquid crystal display of the third embodiment according to the present invention

11—Semiconductor substrate (p-type Si substrate)

12—p-well region
13A to 13C—Field oxide film
14—Switching element (MOSFET)
15—Gate oxide film
16—Gate electrode
17—Drain region
18—Drain electrode
19—Source region
20—Source electrode
21—Diffused capacitor electrode
22—Insulating film
23—Capacitor electrode
24—Capacitor electrode contact
25—First interlayer insulating film
26—First metallic film
27—Second interlayer insulating film
28—First light-blocking metallic film of the first to third embodiments (second metallic film)
29—Third interlayer insulating film
30—Reflective pixel electrode (third metallic film)
31—Antireflection film
32—Light-blocking insulating film
33—Second light-blocking metallic film of the first embodiment
34—Antireflection film
35—Tungsten
36—Light-blocking insulating film
37—Second light-blocking metallic film of the second and third embodiments
38—Light-blocking insulating film
39—Third light-blocking metallic film of the third embodiment
41—Liquid crystal
42—Transparent counter electrode
43—Transparent substrate (glass substrate)
70—Active-matrix drive circuit
71—Horizontal shift register circuit
72—Video switch
73—Signal line
74—Video line
75—Vertical shift register circuit
76—Gate line
C1 to C3—Storage capacitors

D—Drain

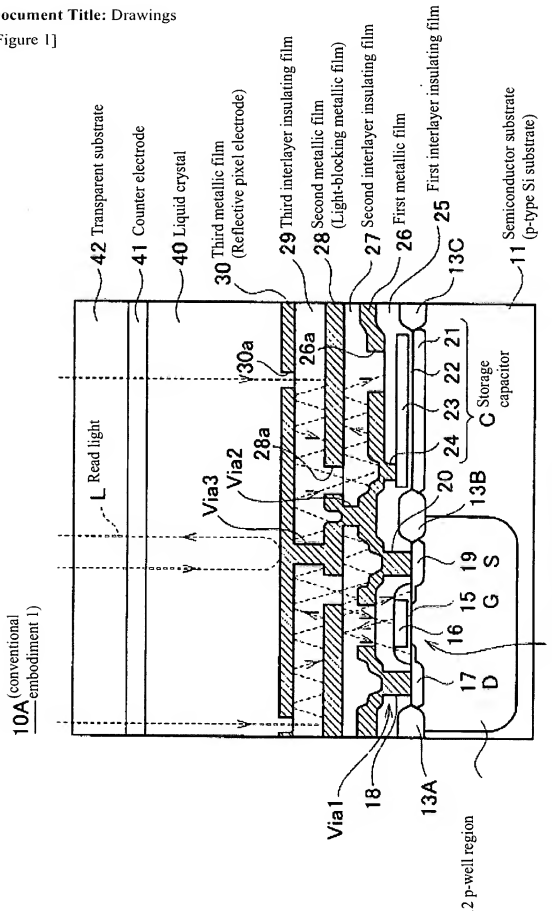
G—Gate

S—Source

Via 1 to Via 3—First to third via holes

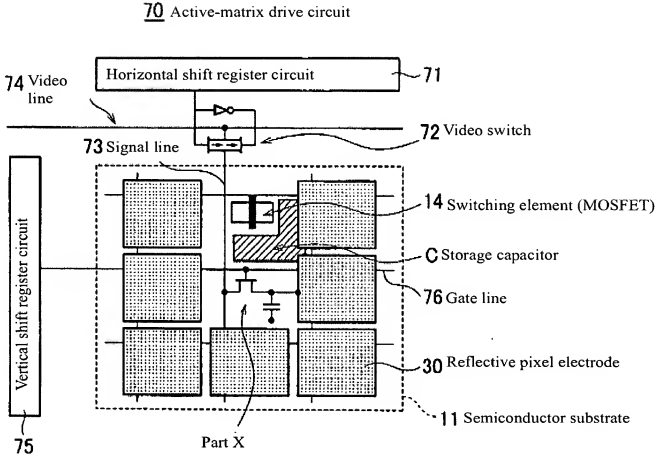
**Document Title:** Drawings

[Figure 1]



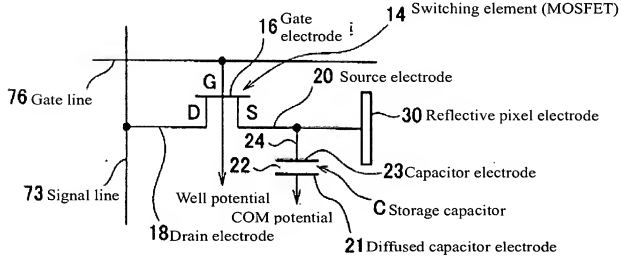
[Figure 2]

(a)

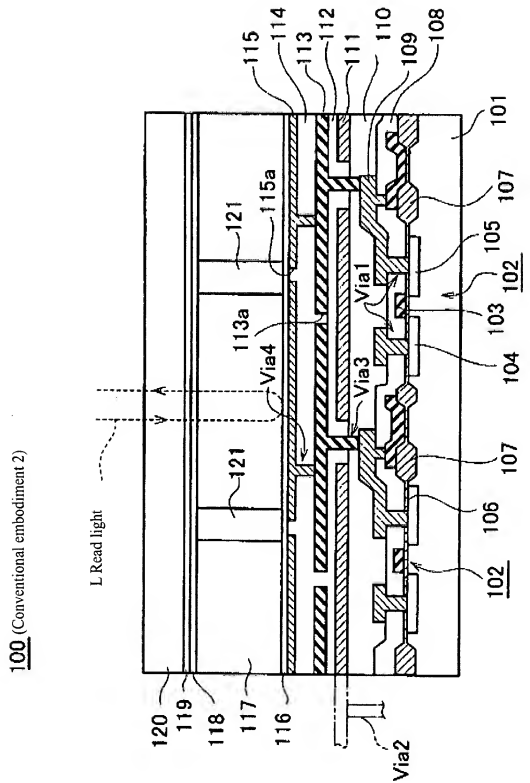



(b)

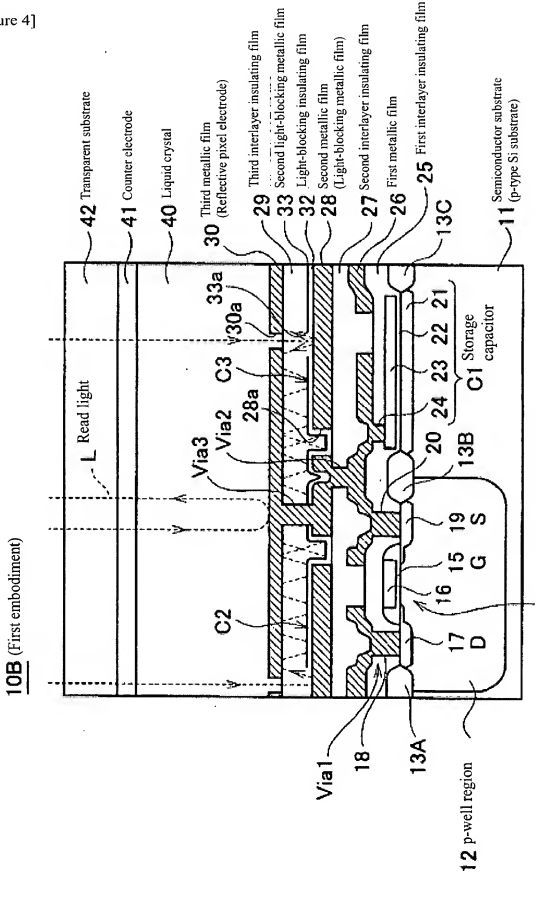
Enlarged view of part X



[Figure 3]

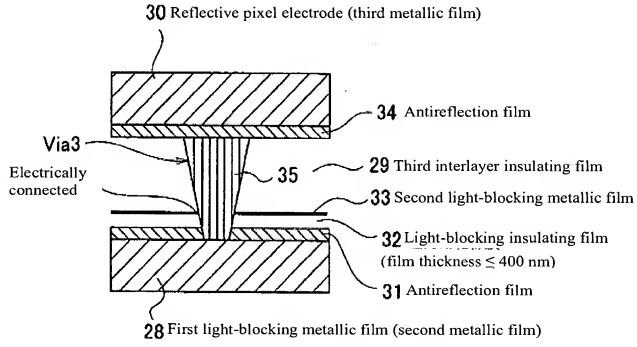

100 (Conventional embodiment 2)
L Read light
120
119
118
117
116
Via2
121
121
113a
115a
Via4
Via3
Via1
115
114
113
112
111
110
109
108
101
107
105
102
103
104
107
106
102

[Figure 4]

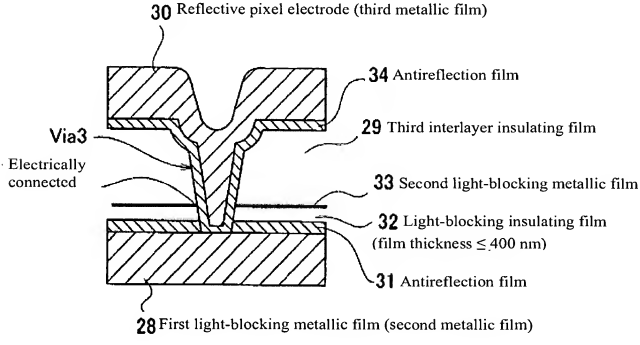

10B (First embodiment)
42 Transparent substrate
41 Counter electrode
40 Liquid crystal
30 Third metallic film (Reflective pixel electrode)
29 Third interlayer insulating film
33 Second light-blocking metallic film
32 Light-blocking insulating film
28 Second metallic film (Light-blocking metallic film)
27 Second interlayer insulating film
26 First metallic film
25 First interlayer insulating film
13C
11 Semiconductor substrate (p-type Si substrate)
L Read light
33a
30a
Via3
Via2
28a
C3
C2
20
13B
24 23 22 21
C1 Storage capacitor
19
15
16
17
D
G
S
14 Switching element (MOSFET)
Via1
18
13A
12 p-well region

[Figure 5]

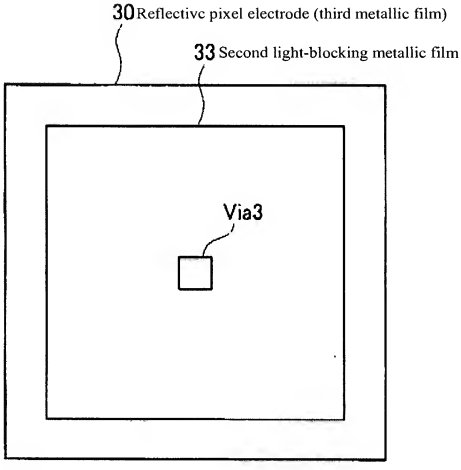
(a) The third via hole inside is formed with tungsten




(b) The third via hole is formed with aluminum wiring

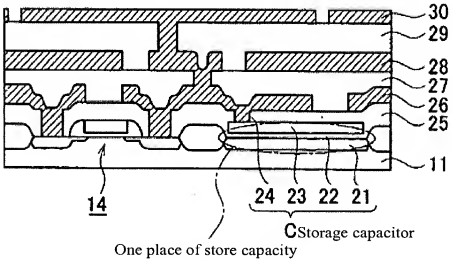


[Figure 6]

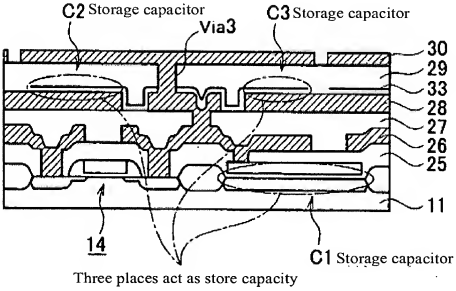

30 Reflective pixel electrode (third metallic film)
33 Second light-blocking metallic film
Via3

[Figure 7]

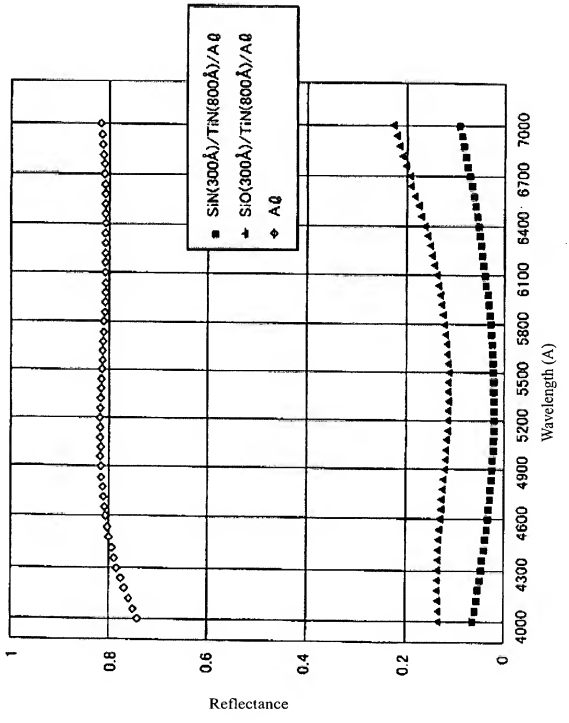
(a) Conventional embodiment 1 as a comparative example




(b) The present invention

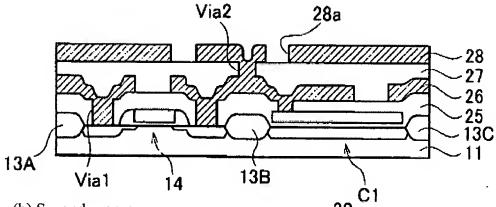


[Figure 8]

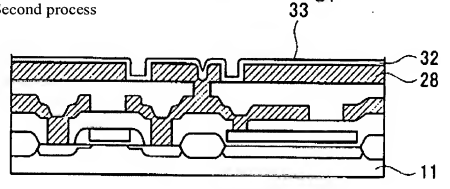

SiN(300Å)/TiN(800Å)/Al
SiO(300Å)/TiN(800Å)/Al
Al
Reflectance
1
0.8
0.6
0.4
0.2
0
4000
4300
4600
4900
5200
5500
5800
6100
6400
6700
7000
Wavelength (A)

[Figure 9]

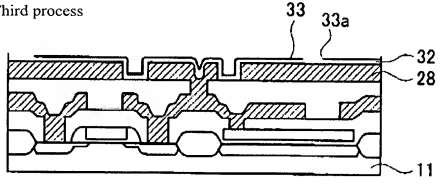
(a) First process



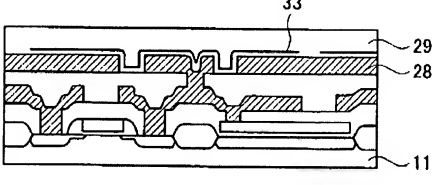

(b) Second process




(c) Third process

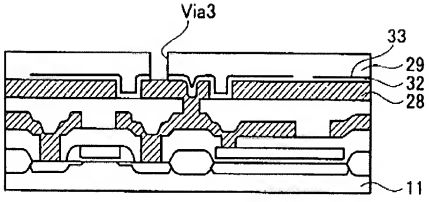



(d) Fourth process

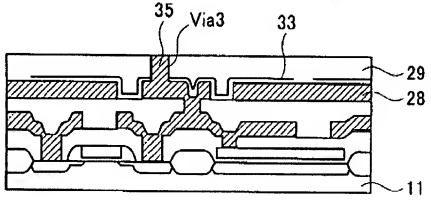


[Figure 10]

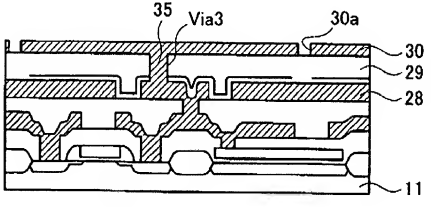
(a) Fifth process



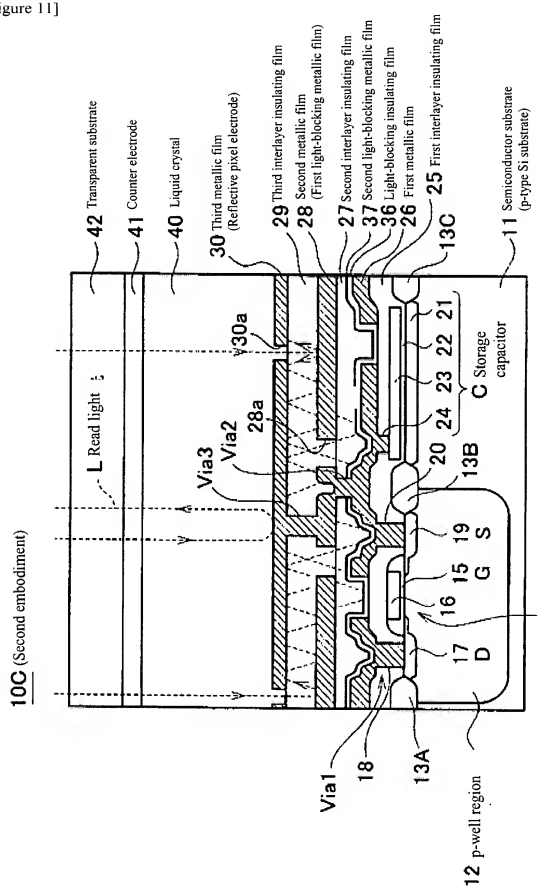

(b) Sixth process



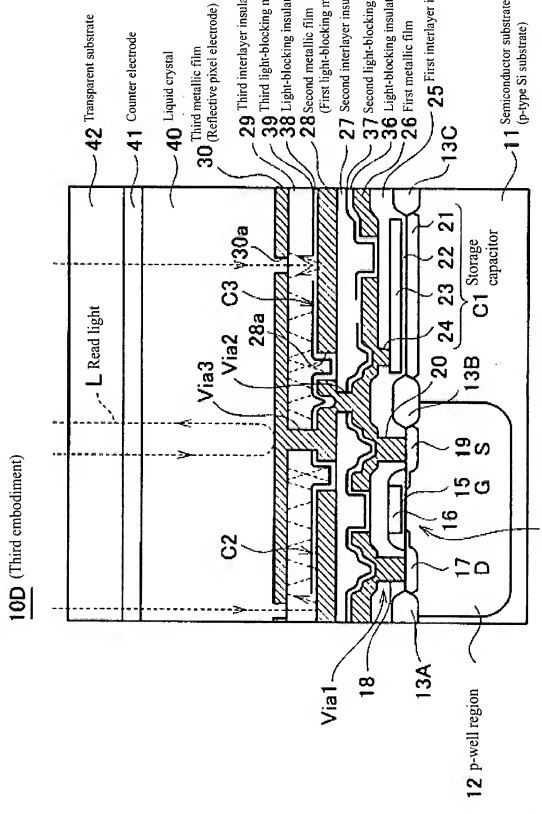

(c) Seventh process



[Figure 11]


10C (Second embodiment)
L Read light
42 Transparent substrate
41 Counter electrode
40 Liquid crystal
30 Third metallic film (Reflective pixel electrode)
29 Third interlayer insulating film
28 Second metallic film (First light-blocking metallic film)
27 Second interlayer insulating film
37 Second light-blocking metallic film
36 Light-blocking insulating film
26 First metallic film
25 First interlayer insulating film
13C
11 Semiconductor substrate (p-type Si substrate)
30a
Via3
Via2
28a
C Storage capacitor
21
22
23
24
20
13B
19
S
15
G
16
D
17
14 Switching element (MOSFET)
Via1
18
13A
12 p-well region

[Figure 12]


10D (Third embodiment)
L Read light
42 Transparent substrate
41 Counter electrode
40 Liquid crystal
30 Third metallic film (Reflective pixel electrode)
29 Third interlayer insulating film
39 Third light-blocking metallic film
38 Light-blocking insulating film
28 Second metallic film (First light-blocking metallic film)
27 Second interlayer insulating film
37 Second light-blocking metallic film
36 Light-blocking insulating film
26 First metallic film
25 First interlayer insulating film
13C
11 Semiconductor substrate (p-type Si substrate)
30a
C3
28a
Via3
Via2
C2
20
13B
24
23
22
21
C1 Storage capacitor
16
15
19
17
D
G
S
14 Switching element (MOSFET)
Via1
18
13A
12 p-well region

**Document Title:** Abstract of the Invention

**ABSTRACT**

**PROBLEM TO BE SOLVED:** To reduce the process of forming a via hole.

**SOLUTION:** A first and second light-blocking metallic films 28, 33 are formed between a semiconductor substrate 11 and a plurality of reflective pixel electrodes 30 by interposing insulating films 27, 32, 29 on and under each layer of the light-blocking metallic films in order to block part of the read light L reaching a switching element 14 when part of the read light L that is made incident from a transparent substrate side 42 to a liquid crystal 40 through a counterelectrode 41 penetrates a third interlayer insulating film 29 passing through an opening 30a formed between the adjacent reflective pixel electrodes 30. One of the first and second light-blocking metallic films 28, 33 covers the opening 30a formed between the adjacent reflective pixel electrodes 30. One of the first and second light-blocking metallic films 28, 33 is electrically connected, through a third via hole Via 3, to one of the switching elements 13, one of the reflective pixel electrodes 30, and storage capacitors C1 to C3.

**Representative drawing:** Fig. 4

Japanese Patent Application 2002-362406

Applicant History Information

Identification numbers [000004329]

1. Date of modification: August 8, 1990

[Reason of modification] Initial registration

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Name: Victor Company of Japan, Limited